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CMOS evolution. Development limits

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Evolution of complementary metal oxide semiconductor (CMOS) technology is presented from the very first MOS transistors to state-of-the-art structures. Difficulties of scaling are discussed together with ways to overcome them. New options for silicon microelectronics (SOI technology and strain engineering) are described. Finally, fundamental limitations to progress in semiconductor devices are considered.

Key words: *CMOS; scaling; silicon microelectronics; silicon on insulator;SOI; strained silicon*

1. Introduction

Global amount of information doubles every year. If the current growth trend is maintained till 2020, this amount will be doubling every two weeks. While it is not the intention of the authors to discuss advantages or disadvantages of this state of affairs, we believe that one of the most important factors that led to such unprecedented growth is semiconductor electronics. We admit that the need for communications and data processing appeared long before the invention of transistor or even before the beginnings of electronics. It should be noted, however, that the development of semiconductor devices plays an extremely important role in information technology.

The slide rule (the majority of the readers have probably never had a chance to use it) was invented in the first half of the 17th century and was widely used for over 300 years. It was even used to design the first microprocessor (Intel 4004). Today's microprocessors have incomparable computing power thanks to the development of silicon microelectronics. It was found many years ago that the temporal behaviour of this development is exponential which is widely known as Moore's law [1]. To be more accurate, the development of practically any area of human activity follows the so called logistic curve. In the beginning, the rate of progress is slow, then thanks to several discoveries an innovations it gains momentum and becomes exponential, finally it slows down due to the lack of knowledge, technical and economic limitations or, possibly, due to a change of interests until an unprecedented breakthrough takes the development to a higher level and the whole process is repeated again (Fig. 1).

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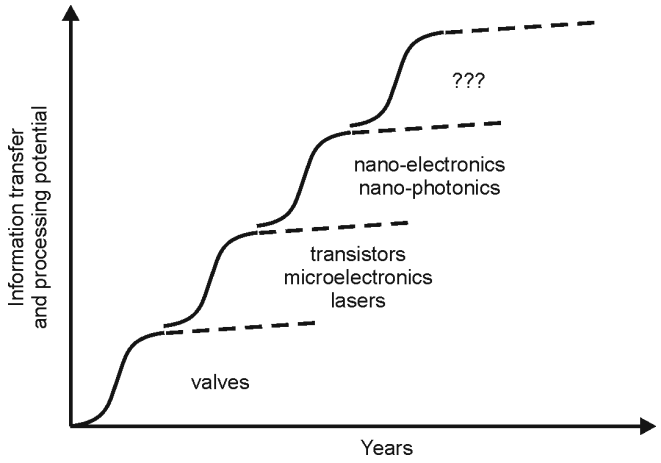

Fig. 1. Development of electronics

To illustrate the rate of exponential development, let us take dynamic random access memory (DRAM) as an example. Its capacity in 1970 was 1 kb, today it is 2 Gb. If we could find a way to multiply our financial means equally fast, during 37 years we would move from $1000 to 2 billion dollars! Obviously, budget planning in each of these two cases is an altogether different matter. With exponential development, a given quantity needs a specific time period to double its value (or to halve it). These periods are listed in Table 1 for several important microelectronics parameters.

Table 1. Examples of exponential development of silicon microelectronics [2]

Parameter	Trend	Period required to double/halve [years]
Average transistor price	decrease	1.6
Price of 1bit of DRAM	decrease	1.5
DRAM feature size	decrease	5.4
Processor performance (MIPS)	increase	2
Microprocessor clock frequency	increase	3
Total bits shipped	increase	1.1
Total transistors shipped	increase	1.5
DRAM capacity	increase	1.6

2. Evolution of MOSFET

Even though microelectronics started with germanium-based devices, silicon soon became its material of choice. This is because it is widely available and much cheaper than other semiconductor materials (see Table 2), it is easily passivated through oxida-

tion and has very good electrical properties. Recently it was found that silicon also has excellent mechanical properties, hence it has found application in microsystems.

Table 2. Prices of semiconductor substrates

Parameter	Material		
	Si	GaAs	InP
Wafer diameter*	12″	6″	4″
Wafer price [a.u.]	1	4	10
Price of 1 mm^2 [a.u.]	1	16	90

*Wafer diameters reflect the state-of-the-art in mass production in 2006.

A vast majority of integrated circuits are produced in CMOS technology. This technology is based on a pair of complementary MOSFETs (n-channel transistor and p-channel transistor). A schematic cross-section of a modern MOSFET is shown in Fig. 2.

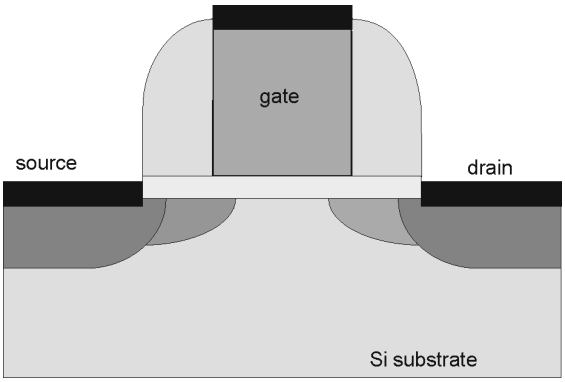

Fig. 2. A cross-section of a modern MOSFET

The principle of operation of this device is rather simple. If a sufficiently high positive voltage is applied to the gate, electrons are attracted to the semiconductor surface and a conductive channel is formed between source and drain making current flow possible. Gate voltage necessary to form the channel is called the threshold voltage V_T. According to the simplest theory of MOSFET, its most important parameters, that is drain current $I_{D\mathrm{sat}}$ and transconductance in saturation $g_{m\mathrm{sat}}$, may be described in the following way:

$$I_{D\mathrm{sat}} = \frac{W}{2L}\mu_{\mathrm{eff}} C_{\mathrm{diel}} \left(V_{GS} - V_T\right)^2 \tag{1}$$

$$g_{m\mathrm{sat}} = \frac{\partial I_{D\mathrm{sat}}}{\partial V_{GS}} = \frac{W}{L}\mu_{\mathrm{eff}} C_{\mathrm{diel}} \left(V_{GS} - V_T\right) \tag{2}$$

where: W, L are channel width and length, respectively, μ_{eff} is effective carrier mobility in the channel, C_{diel} – gate-dielectric capacitance per unit area, and V_{GS} stands for gate-to-source voltage.

To complete the description of MOSFET operation, a formula for cut-off frequency f_{T} is needed:

$$f_T = \mu_{\text{eff}} \frac{V_{GS} - V_T}{L^2} \tag{3}$$

In view of the above equations, the most obvious way to increase all these parameters would be to reduce channel length. If L is reduced 5 times it would be expected that the current will be five times higher at the same supply voltage, therefore a reduction of this voltage could be envisaged. The reduction of channel length upon time is shown in Fig. 3. It should be noticed that L decreased almost 3 orders of magnitude in approximately 30 years.

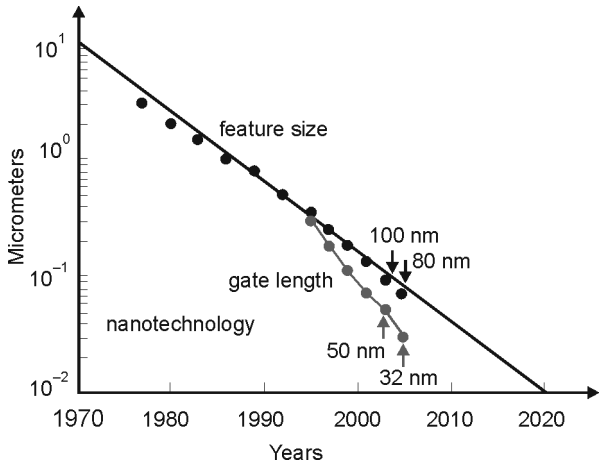

Fig. 3. Miniaturization of a semiconductor devices with time

This trend may be approximately described as:

$$L = 10\exp\left[-0.14\left(\text{year} - 1970\right)\right] \quad [\mu\text{m}] \tag{4}$$

In practice, however, reducing the channel length is not simple. Already in early seventies, when channel length of 1 μm was considered very short, it was found that drain field penetrates into the channel region which should normally be controlled by the gate, leading to lower threshold voltage values, especially at high drain voltages. Extensive studies indicated that to minimize this undesirable effect, the reduction of horizontal dimensions must be accompanied by an appropriate reduction of vertical ones (gate dielectric thickness and junction depth), increased doping and lowered supply voltage [3]. In fact, the evolution of MOSFET is a battle against so called

short-channel effects (SCE). A detailed history of MOSFET was presented in [4]. Here only a brief outline is given. Innovations implemented in MOSFET architecture are schematically illustrated in Fig. 4. The concept of a MOS structure was invented by Lilienfeld [5] in the late twenties. A great technological step towards today's MOSFETs was development of the silicon surface stabilization method by means of oxidation [6]. The first silicon MOSFET was presented in [7]. Not much later the concept of a CMOS inverter was invented [8]. Early MOSFETs had aluminum gate (Fig. 4a). Development of poly-Si gate [9] led to a self-aligned device (Fig. 4b), where the gate itself constitutes a mask for source and drain diffusion. In this way parasitic gate-to-source and gate-to-drain capacitances associated with gate overlap could be controlled.

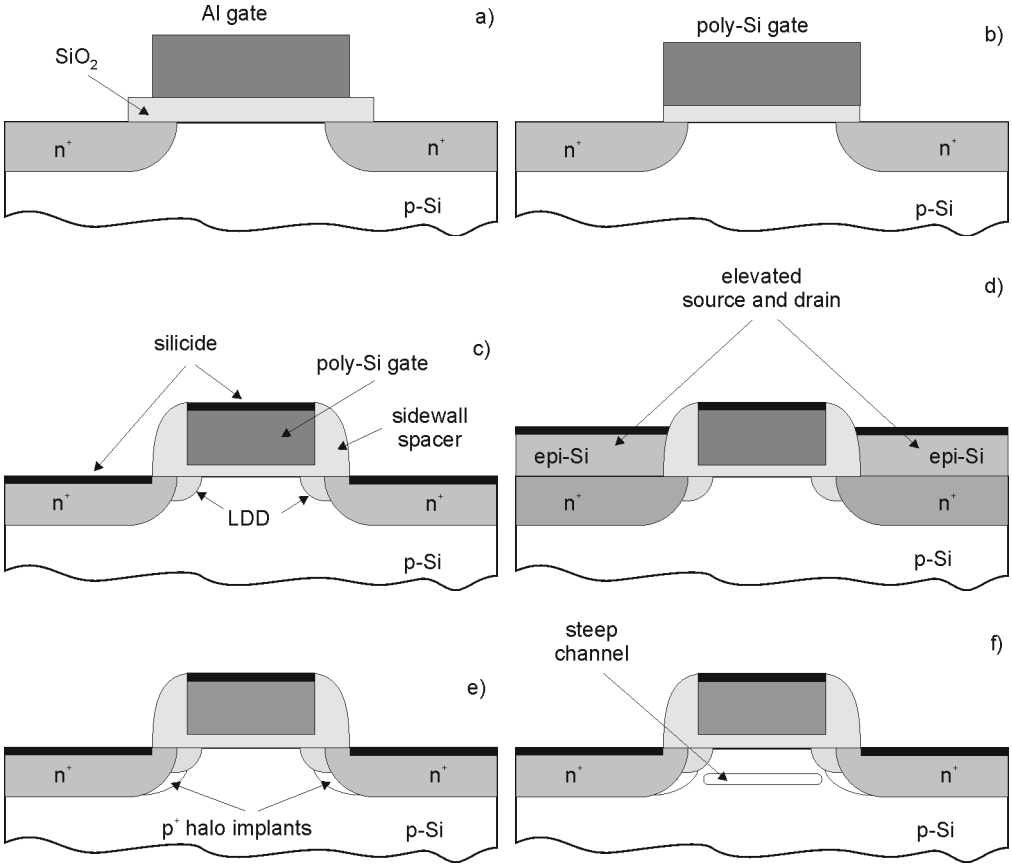

Fig. 4. Changes in MOSFET architecture: a) Al gate, b) self-aligned poly-Si gate, c) LDD structure with a silicided gate, source and drain, d) raised source and drain, e) halo implants, f) steep retrograde doping profile in the channel

As mentioned before, the main problem that appeared with the reduction of channel length was the short-channel effects (SCE). These undesirable phenomena are

caused by the fact that gate control over the channel is reduced by the influence of the drain potential (charge sharing). The most obvious result of this situation is that threshold voltage becomes dependent on channel length. One of the first models describing length-dependent threshold voltage was presented in [10]. Another short channel effect (the so called drain-induced barrier lowering DIBL [11]) is associated with interaction between source-channel barrier and drain potential. In long-channel devices this barrier is controlled by the gate. As the channel length is decreased, the drain potential affects the barrier, making threshold voltage dependent also on drain bias. Finally, as source and drain get closer, the risk of punch-through increases. Attempts made to minimize short channel effects concentrated on three different regions of the transistor, that is the source/drain, gate stack and channel.

2.1. Source/drain engineering

Control of SCE requires the reduction of source/drain junction depth [12]. This, however, increases the resistance of those regions, especially since doping concentration cannot exceed solid solubility limits. The first attempt to cope with this problem was lightly doped drain (LDD) together with spacer technology [13] (Fig. 4c). The shallow, lightly doped part of the drain served to reduce the maximum electric field. The deeper heavily doped part minimized the resistance. The spacer helped to control gate overlap holding parasitic capacitance in check. A further reduction of S/D resistance may be obtained through silicidation (Fig. 4c). Another way to reduce the parasitic resistance is to use elevated sources and drains (Fig. 4d) where the thickness of S/D regions is increased by selective Si epitaxy [14]. An ultimate solution to the problem might be the Schottky barrier S/D [15].

2.2. Channel engineering

Channel engineering is mostly intended to control threshold voltage and prevent punch-through. Increasing channel doping reduces the width of the depletion region thus minimizing SCE, it has however a deleterious effect on the mobility (e.g., [16]). Halo (pocket) implants were introduced [17] to control short channel effects by reducing the width of the depletion region and to increase device resistance to punch-through (Fig. 4e). A super-steep retrograde doping profile [18] in the channel serves for a better control of threshold voltage while keeping mobility high due to low surface doping (Fig. 4f).

2.3. Gate stack engineering

The structure of a gate stack is schematically shown in Fig. 5. Even highly doped, the poly-Si gate electrode represents a certain resistance. Deposition of a refractory metal silicide (the so called polycide) on top of the gate [19] helps alleviate this problem

(Fig. 4c). Gates made entirely of such silicides were also considered (e.g., [20, 21]). Self-aligned silicidation (salicidation) [22] made it possible to form silicide in selected regions (gate and S/D) without lithographic patterning. Another problem with poly-Si gates is depletion near the gate dielectric. Heavy doping reduces this effect but still in the on-state the equivalent gate oxide thickness (EOT) is increased by 0.4–0.5 nm. Slightly better results are obtained using poly-SiGe. It seems that metal gates will be the ultimate solution to this problem.

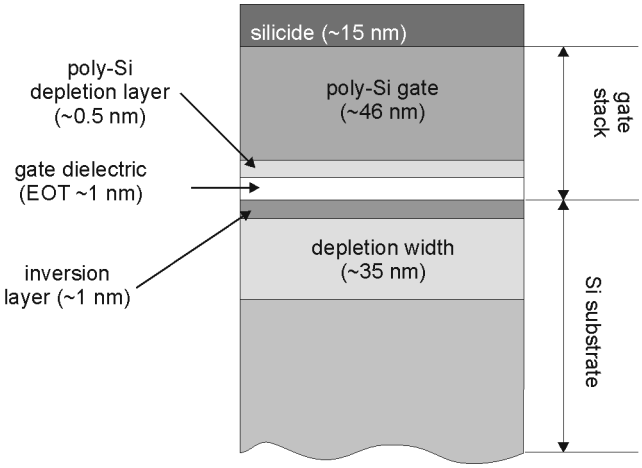

Fig. 5. Gate-stack structure

As seen from Eqs. (1) and (2), the reduction of gate-oxide thickness (increasing C_{diel}) results in higher current and transconductance. This is because the gate has better control of the channel. Changes of gate-oxide thickness over the years are shown in Fig. 6.

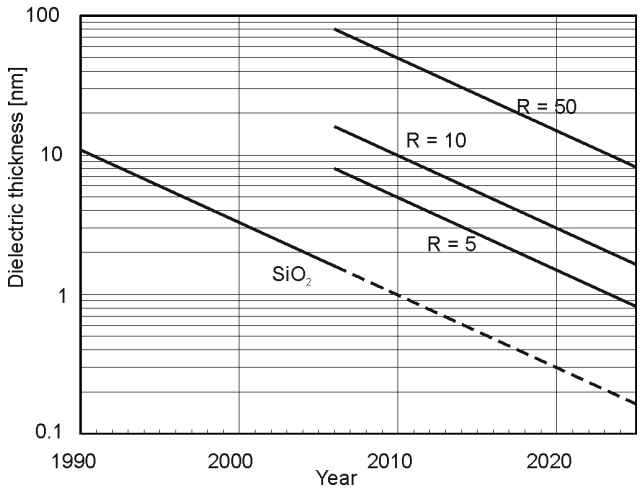

Fig. 6. Temporal evolution of the gate-oxide thickness

In an approximate way this trend may be described as:

$$t_{ox} = 120 \exp\left[-0.12\left(\text{year} - 1970\right)\right] \quad \text{[nm]} \tag{5}$$

As a result of decreased thickness, gate leakage current obviously grows, increasing power consumption of the entire chip, which is an undesirable effect for battery-powered mobile systems. It is estimated that gate leakage current increases approximately 30 times every technology generation, as opposed to 3–5 times increase of channel leakage current [23]. Apart from leakage current, the reduction of gate-oxide thickness increases the susceptibility of the device to boron penetration from the poly-Si gate into the channel. Replacing silicon dioxide with oxynitride (SiO_xN_y) is the most widely used solution to this problem (e.g., [24]). Eventually, however, oxynitride will have to give in to high-*k* dielectrics. If we assume that *R* is the ratio of the electric permittivity to that of SiO_2, then the layer of this dielectric may be *R* times thicker than SiO_2 and still produce the same capacitance at much lower leakage. The thickness of hypothetical materials with various values of *R* is plotted versus time in Fig. 6. Unfortunately, materials that might replace SiO_2 in the future have to meet several other requirements, such as resistance to thermal processing, low density of interface traps, sufficiently wide bandgap, etc. It seems that the gate dielectric will have to consist of two layers: a very thin buffer layer of SiO_2 to maintain high quality of the dielectric –semiconductor interface and a layer of high-*k* dielectric (Fig. 7). In the latter case, HfO_2 is believed to be the most promising candidate.

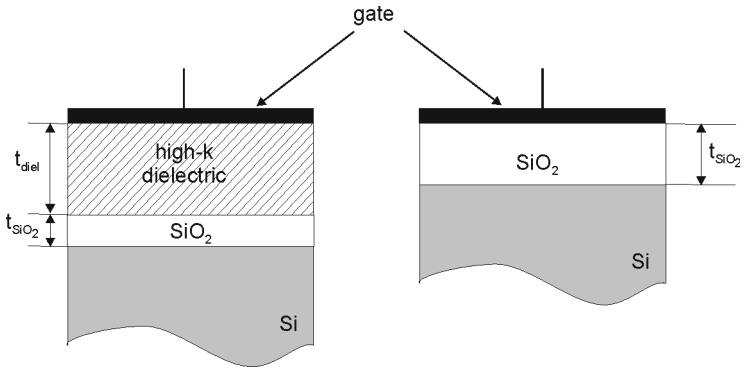

Fig. 7. Dual gate dielectric structure (left) compared to the standard structure (right)

2.4. Other scaling problems

Transport models used to describe semiconductor devices are usually developed with the assumption that device dimensions are much larger than the carrier free path. If this assumption is not justified, one has to deal with ballistic transport [25]. Moreover, progressing miniaturization causes device active regions to become ever smaller, therefore the number of dopant atoms in these regions decreases, too (Table 3). Thus

statistical fluctuations of doping concentration will become a challenge for process repeatability.

Table 3. Decreasing number of dopant atoms in the active region of a MOSFET

Parameter	Yesterday	Today	Tomorrow
Doping concentration [cm^{-3}]	10^{16}	10^{18}	10^{19}
Channel length [μm]	10	0.1	0.01
Channel width [μm]	10	0.25	0.01
Depletion width [μm]	0.3	0.03	0.002 (SOI)
Number of dopant atoms in the depletion region	3×10^{15}	750	2

3. Future progress

For the past 40 years the progress in silicon microelectronics was achieved mainly through miniaturization of both horizontal and vertical dimensions of the transistor. It seems, however, that this trend has to be accompanied by additional innovations to ensure the same rate of progress. It is believed [26] that there are four directions to follow: increasing inversion charge at constant voltage drive (i), improving carrier transport (ii), choosing 'scaling-friendly' device architectures to obtain shorter channels (iii) and reducing parasitic resistance and capacitance (iv).

3.1. Silicon on insulator

Silicon-on-insulator (SOI) technology [27] is the first step in the directions (i), (iii) and (iv). In this technology, the active region of a MOSFET is separated from the bulk

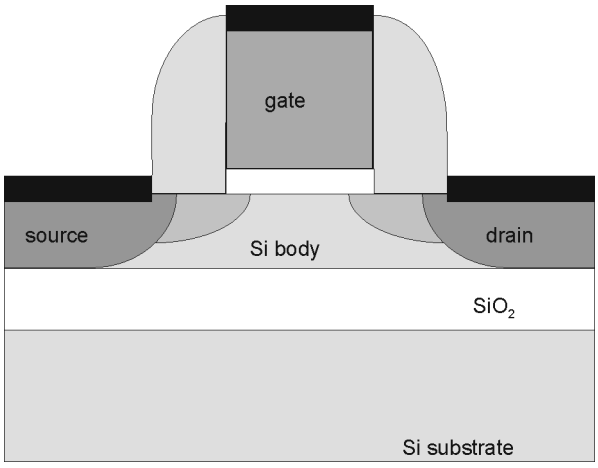

Fig. 8. Cross-section of a SOI MOSFET

silicon by a layer of buried oxide (BOX). A cross-section of a SOI device is shown in Fig. 8. The advantage of SOI is the ease of electrical insulation of a device from the rest of the integrated circuit, which increases packing density. Moreover, the areas of source and drain junctions are significantly reduced, thus decreasing parasitic capacitances. Finally, the depletion width is limited by the Si body thickness; therefore it is widely believed that SOI helps to reduce short channel effects (SCE) unless source-to-drain coupling through channel and BOX cannot be neglected. Properties of SOI devices are improved with the reduction of body thickness. It is believed that fully depleted ultra-thin-body SOI (FD UTB SOI) is one of the best scaling solutions. Due to excellent gate control of the channel, these devices may be undoped or very lightly doped. In this way, mobility is not degraded and threshold voltage is less dependent on the fluctuations of doping concentration [28].

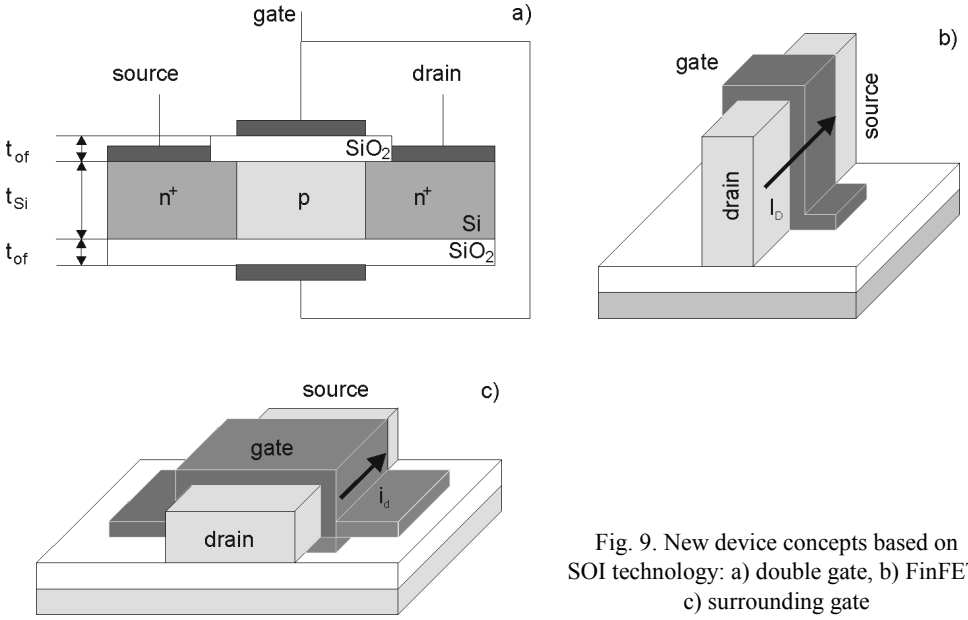

Fig. 9. New device concepts based on SOI technology: a) double gate, b) FinFET, c) surrounding gate

Another advantage of SOI is that it facilitates development of new device concepts. The first of those is the double-gate transistor (DG) shown schematically in Fig. 9a. Due to the presence of two gates, the influence of the longitudinal field induced by drain bias on the source-end of the channel is reduced [29], thus decreasing SCE. On the other hand, fabrication of these devices is not easy, especially alignment of the gates to one another and self-alignment of source and drain regions to both gates. These technological problems are considerably eased with a FinFET (Fig. 9b). A natural step forward is a transistor with a surrounding gate (e.g., [30]), presented in Fig. 9c. The ultimate surrounding-gate transistor is shown in Fig. 10. The geometry of a silicon nanowire makes gate control of the channel the highest possible.

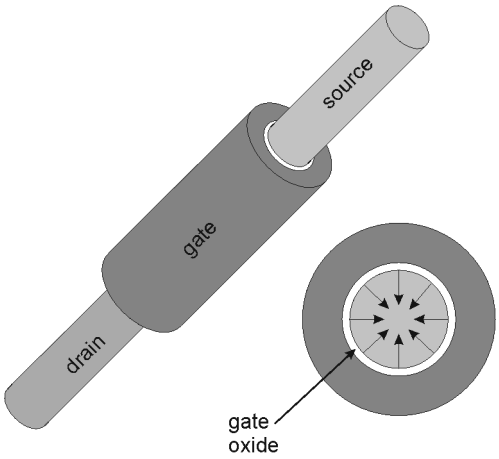

Fig. 10. Ultimate surrounding gate MOSFET

Due to undoped channels, the gate current is greatly reduced in FD UTB SOI and FinFETs [23] but the source-to-drain current in the off-state is not minimized easily. In Figs. 11a and 11b predictions of both these currents over the years are shown [31].

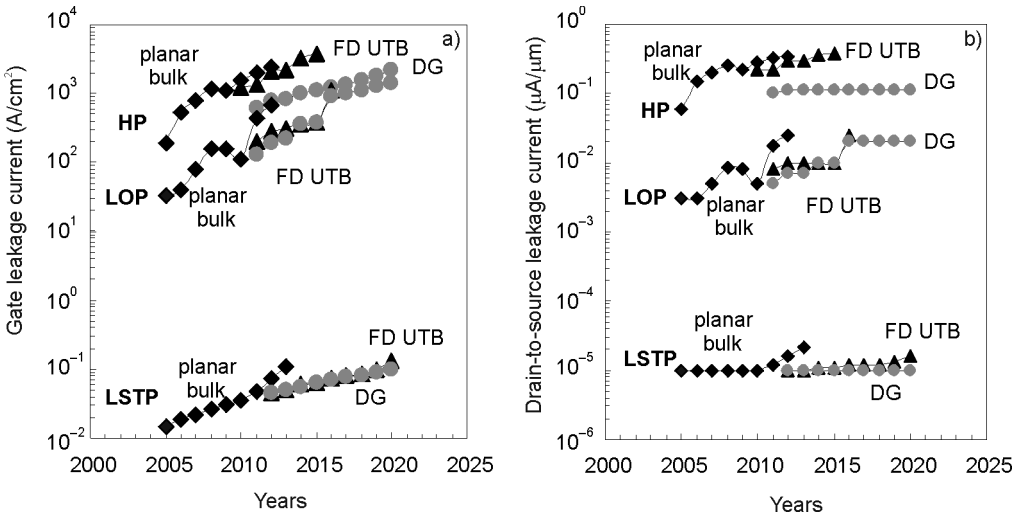

Fig. 11. Prediction [31] of gate leakage current (a) and source-to-drain current (b) for three application types: HP – high performance, LOP – low operation power, LSTP – low standby power

Unfortunately, as all human inventions, SOI technology is not perfect. One of its biggest problems is self-heating. Thermal conductivity of the buried oxide (1.4 $W \cdot m^{-1} \cdot K^{-1}$) is almost a hundred times lower than that of bulk Si (120 $W \cdot m^{-1} \cdot K^{-1}$). As a result, the mobility is lowered. Scaling of Si body thickness degrades thermal conductivity even further [23].

3.2. Stress engineering

While SOI technology is certainly a big step forward towards better devices, it does nothing to enhance transport properties. Carrier transport may be improved either using a high-mobility material in the channel (e.g. Ge, GaAs, etc.) or changing the properties of silicon by means of stress. Stress is introduced in the device using either a global technique (across the entire substrate) or a local one (based on epitaxial layers or high-stress cappings) [32]. The global approach consists, in, e.g., depositing a thin layer of silicon on a relaxed SiGe substrate (Fig. 12).

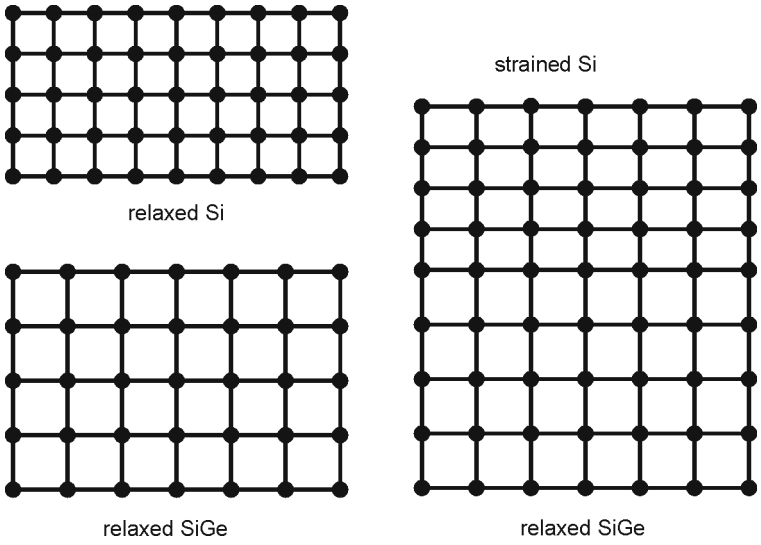

Fig. 12. Strained silicon on SiGe

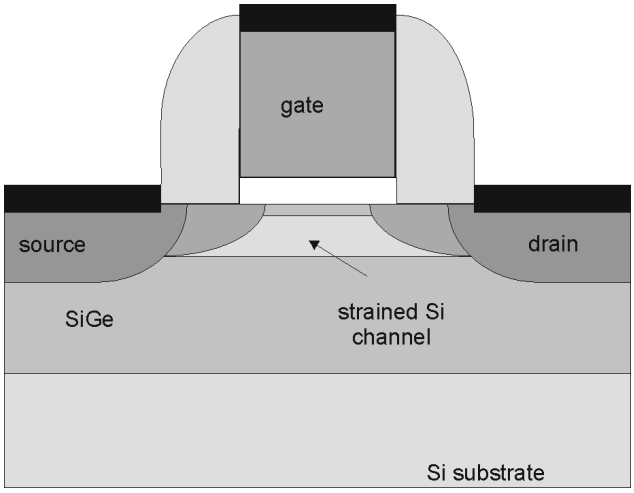

Fig. 13. MOSFET with a strained-silicon channel

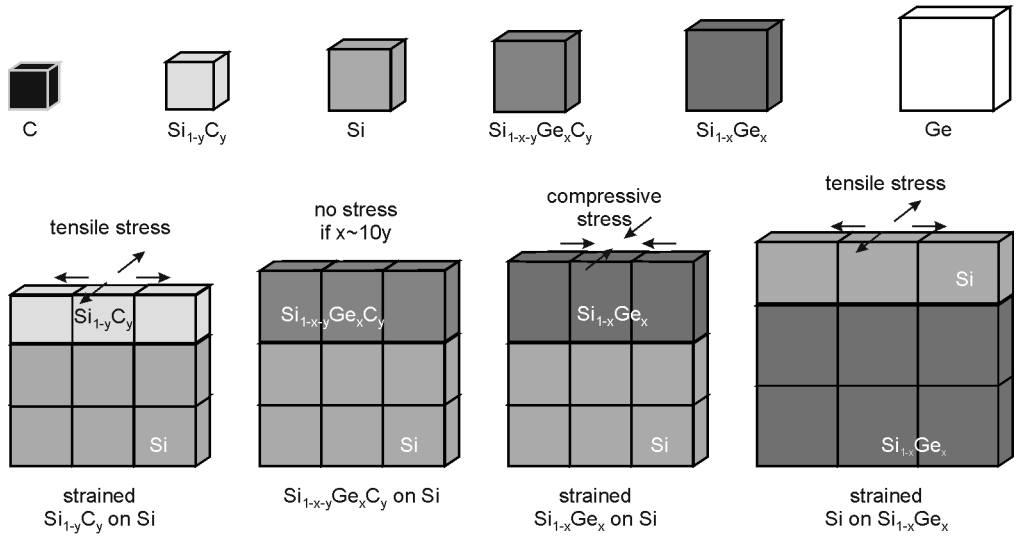

Fig. 14. Stress engineering – material combinations

Due to a lattice mismatch between SiGe and Si, the obtained silicon layer is strained improving electron mobility. A cross-section of a transistor with strained Si channel obtained by means of a global technique is shown in Fig. 13. Other material combinations that may be used for stress engineering are shown in Fig. 14. Local techniques include source and drain stressors (filling etched parts of source and drain with epitaxial SiGe for n-channel or SiC for p-channel devices) and deposition of highly tensile (Si_3N_4) or compressive (SiN) capping layers over complete devices. These techniques may also be combined to further improve transport properties.

4. Fundamental limitations

Fundamental limitations are often studied using a classical example of an ultimate laptop with the mass of 1 kg and volume of 1 dm^3 [33]. An elementary logic operation performed during time period Δt requires an average energy expense E determined from Heisenberg's uncertainty principle:

$$E \geq \frac{\pi\hbar}{2\Delta t} \tag{6}$$

As a result, a system with an average energy E may perform no more than $2E/\pi/\hbar$ logic operations during Δt. If, therefore, a 1-kg laptop has the energy of:

$$E = mc^2 = 8.9874 \times 10^{16} \text{ J} \tag{7}$$

it is capable of performing no more than 5.4×10^{50} operations per second. This simple calculation (its result is independent of computer architecture) indicates that we have

more than 200 years to go before this limitation kicks in, assuming that the current development rate (described by Moore's law) will be maintained in the future. It should be remembered though that modern computers contain many parts the mass of which cannot be transformed into data-processing energy. If we remember that energy determines velocity and entropy determines capacity (memory), another calculation leads to the conclusion that our ultimate laptop may contain up to approximately 2×10^{31} bits of memory. Other conclusions resulting from this analysis are less optimistic. The dissipated power and temperature of our computer are at the level of a huge nuclear explosion [33].

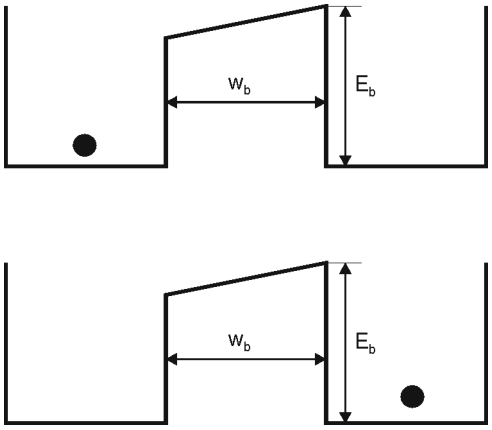

Fig. 15. Schematic illustration of a potential barrier in a switching device

Here is another simple analysis. Let us imagine that a bit of information is a charge carrier in a potential well. This well is separated from another one by a potential barrier E_b (Fig. 15). The classical probability of a carrier passing over the barrier is:

$$P = \exp\left(-\frac{E_b}{kT}\right) \tag{8}$$

According to the Shannon–von Neumann–Landauer expression, for both states to be distinguishable ($P < 1/2$) the barrier height must be at least:

$$E_b > kT\ln 2 \tag{9}$$

Let us assume that energy $E_b = 10kT$ is necessary to ensure that both states may be distinguished. If we use the uncertainty principle again, the time necessary to perform a logic operation is $\Delta t = 4\times10^{-15}$ s. If we assume further that our hypothetical switching device has the size of 5 nm×5 nm (considering recent progress in CMOS technology, such an assumption does not seem to be overly optimistic), the number of such devices packed in the area of 1 cm^2 is $N = 4\times10^{12}$. The power density is therefore:

$$P \approx N\times\frac{10kT}{\tau} \approx 4\times10^{7}\ \text{W/cm}^2 \tag{10}$$

It seems that heat removal will be the main scaling problem in the future. It will be more or less equally critical for any devices based on electron transport intended for digital logic [34]. Thus CMOS technology is still worth some effort. Moving beyond the above mentioned limitations requires considering of completely different physical principles of device operation.

5. Summary

Further scaling of silicon devices will most likely require new materials (e.g. strained silicon), and new device concepts (multi-gate structures enabled by SOI technology). We are confident that CMOS will overcome the difficulties it is facing. During the past 40 years the end of silicon microelectronics had been announced many times and never happened. Silicon technology needs enhancement, though (Fig. 16).

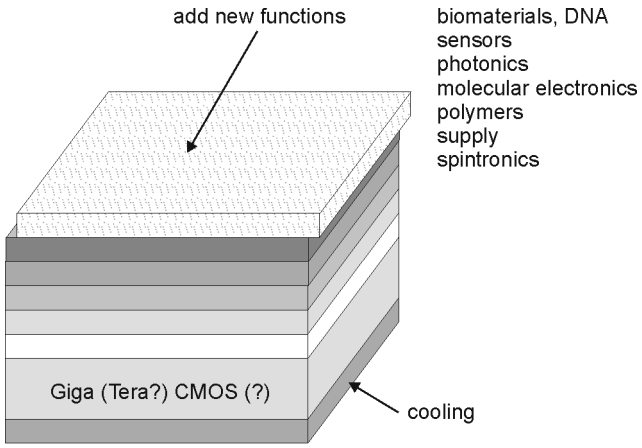

Fig. 16. Integration of silicon microelectronics with other technological solutions

It would be useful to integrate with new technological solutions (or new materials) to improve the functionality of the end product, e.g. silicon micromechanics, cooling systems, optical connections, molecular electronics or even spintronics.

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